**What is claimed is:**

1. A bus interface driver circuit, the circuit comprising:

an external termination pad configured to be coupled to a bus line, the bus line having a termination voltage and a termination impedance;

a first comparator circuit configured to compare the termination voltage to a first reference voltage in order to generate a second reference voltage;

a first current source circuit configured to receive the second reference voltage and generate a reference current that corresponds to the second reference voltage;

a driver circuit configured to receive the reference current and a data signal, where the driver circuit is configured to modulate the reference current responsive to the data signal in order to generate an output current at the external termination pad;

a second comparator circuit configured to compare the termination voltage to the first reference voltage in order to generate a third reference voltage and further compare the third reference voltage to an output voltage at the external termination pad in order to generate a current control signal; and

a second current source configured to receive the current control signal and generate an on-die termination current corresponding to the current control signal at the external termination pad.

2. The bus interface driver circuit of claim 1, where the first comparator circuit further comprises:

a first operational amplifier having first and second input terminals and an output terminal, the first input terminal of the first operational amplifier being coupled

to a circuit node configured to have one of the terminating voltage and the first reference voltage and where the output terminal of the first operational amplifier is coupled to the second input terminal of the first operational amplifier; and

a resistance circuit coupled between the second input terminal of the first operational amplifier and another circuit node configured to have another one of the terminating voltage and the first reference voltage.

3. The bus interface driver circuit of claim 1, where the resistance circuit further comprises a first resistor in series with a selectable resistance circuit.

4. The bus interface driver circuit of claim 2, where the first current source circuit further comprises:

a first transistor having first and second current terminals and a control terminal, where the control terminal of the first transistor is coupled to the output of the first comparator and the second current terminal of the first transistor is coupled to the second input terminal of the first comparator;

a second transistor having first and second current terminals and a control terminal, where the control terminal of the second transistor is coupled to the second current terminal of the second transistor, the second current terminal of the second transistor is coupled to the first current terminal of the first transistor, and the first current terminal of the second transistor is coupled to a circuit node configured to have one of the terminating voltage and a first supply voltage; and



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a third transistor having first and second current terminals and a control terminal, where the control terminal of the third transistor is coupled to the control terminal of the second transistor, the first current terminal of the third transistor is coupled to the circuit node configured to have one of the terminating voltage and a first supply voltage, and the second current terminal of the second transistor is configured to generate the reference current.

5. The bus interface driver circuit of claim 2, where the driver circuit further comprises a differential amplifier having a current supply terminal for receiving the reference current, a non-inverting output coupled to the external termination pad, and an inverting output coupled to another external termination pad configured to be coupled to another bus line, a first input for receiving the data signal and a second input for receiving an inverted data signal, where the differential amplifier is configured to modulate the reference current in a complementary manner responsive to the data signal and the inverted data signal in order to generate the output current at the non-inverting output and an inverted output current at the inverted output.

6. The bus interface driver circuit of claim 5, where the differential amplifier further includes:

a first pair of cross-coupled transistors coupled between the non-inverting output of the amplifier and a ground supply rail, where a first transistor of the first pair is configured to receive the reference current as modulated by the data signal and



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the second transistor of the first pair is larger than the first transistor of the first pair by a predetermined ratio; and

a second pair of cross-coupled transistors coupled between the inverting output of the amplifier and the ground supply rail, where a first transistor of the second pair is configured to receive the reference current as modulated by the inverted data signal and the second transistor of the second pair is larger than the first transistor of the second pair by the predetermined ratio.

7. The bus interface driver circuit of claim 5, where the differential amplifier further includes:

a first complex impedance coupled between the non-inverting output of the amplifier and a control terminal of the second transistor of the first pair; and

a second complex impedance coupled between the inverting output of the amplifier and a control terminal of the second transistor of the second pair.

8. The bus interface driver circuit of claim 2, where the driver circuit further comprises a single ended amplifier having a current supply terminal for receiving the reference current, a non-inverting output coupled to the external termination pad, and a first input for receiving the data signal, where the single ended amplifier is configured to modulate the reference current responsive to the data signal in order to generate the output current at the non-inverting output.



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9. The bus interface driver circuit of claim 8, where the single ended amplifier further includes a pair of cross-coupled transistors coupled between the non-inverting output of the amplifier and a ground supply rail, where a first transistor of the pair is configured to receive the reference current as modulated by the data signal and the second transistor of the pair is larger than the first transistor of the pair by a predetermined ratio.

10. The bus interface driver circuit of claim 9, where the single ended amplifier further includes a complex impedance coupled between the non-inverting output of the amplifier and a control terminal of the second transistor of the pair.

11. The bus interface driver circuit of claim 1, where the second comparator circuit further comprises:

a second operational amplifier having first and second input terminals and an output terminal, the first input terminal of the second amplifier being coupled to a circuit node configured to have one of the terminating voltage and the first reference voltage;

a first resistor coupled between the second input terminal of the second operational amplifier and another circuit node configured to have another one of the terminating voltage and the first reference voltage;

a resistance circuit coupled between the output terminal of the second operational amplifier and the second input terminal of the second operational amplifier;



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a third operational amplifier having first and second input terminals and an output terminal, the first input terminal of the third amplifier being coupled to the output terminal of the second operational amplifier and the second input of the third being coupled to the external termination pad; and

a current logic control circuit having an input terminal coupled to the output terminal of the third operational amplifier and an output terminal for outputting the current control signal, where the current logic control circuit is configured to transform an output signal from the third operational amplifier into the current control signal in a form suitable for driving the second current source.

12. The bus interface driver circuit of claim 11, where:

the current control signal further comprises a digital signal having a plurality of bit lines;

the second current source further comprises a plurality of transistors, each coupled between a circuit node, the circuit node being configured to have one of the terminating voltage and a supply voltage, and the external termination pad and each having a control terminal coupled to a corresponding one of the plurality of bit lines of the current control signal; and

the current logic circuit is configured to drive each one of the plurality of bit lines of the current control signal responsive to the output of the third operational amplifier to selectively activate the plurality of bit lines of the current control signal in order to generate the on-die termination current.



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13. The bus interface driver circuit of claim 11, where:

the current control signal further comprises an analog signal;

the second current source further comprises a plurality of transistors, each coupled between a circuit node, the circuit node being configured to have one of the terminating voltage and a supply voltage, and the external termination pad and each having a control terminal coupled to the output of the current logic circuit; and

the current logic circuit is configured to drive each of the plurality of transistors of the second current source in a linear operating range responsive to the output of the third operational amplifier in order to generate the on-die termination current.

14. The bus interface driver circuit of claim 11, where the second comparator circuit further includes:

a transmit pipeline circuit configured to transmit a predetermined data pattern at the external termination pad responsive to a transmit clock signal, the predetermined data pattern alternating between high and low logic voltage levels;

a receive pipeline configured to receive, responsive to a receive clock signal, a data pattern at the external termination pad corresponding to the predetermined data pattern transmitted by the transmit pipeline circuit;

a comparator configured to compare the received data pattern to the predetermined data pattern in order to generate a counter control signal configured to increase and decrease the current control signal according to the comparison between the received data pattern and the predetermined data pattern.



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15. A method for interfacing to a bus, the method comprising the steps of:

providing an external termination pad configured to be coupled to a bus line;

tracking a difference between a terminating voltage for the bus and a first reference voltage for the bus to produce a second reference voltage;

generating a reference current that corresponds to the second reference voltage;

sourcing the reference current to an amplifier;

amplifying a data signal with the amplifier to drive the external termination pad;

generating a current control signal by comparing a voltage at the external termination pad to the second reference voltage; and

sourcing an on-die termination current to the external termination pad that corresponds to the current control signal.

16. The method of claim 15, where the step of tracking a difference between a terminating voltage for the bus and a first reference voltage for the bus to produce a second reference voltage further comprises:

scaling one of the terminating voltage and the first reference voltage using a resistance circuit;

comparing another of the terminating voltage and the first reference voltage to the scaled one to obtain a difference signal; and



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where the step of sourcing the reference current to an amplifier includes driving a current source with the difference signal through the resistance circuit to the one of the terminating voltage and the first reference voltage.

17. The method of claim 16, where the method includes the step of controlling an output swing of the amplifier by providing a selectably adjustable resistance in the resistance circuit.

18. The method of claim 16, where the step of sourcing the reference current to an amplifier includes mirroring the current through the current source to produce the reference current.

19. The method of claim 15, where the step of amplifying a data signal with the amplifier to drive the external termination pad includes the steps of:

modulating the reference current with the data signal to produce a modulated current signal;

sinking the modulated current signal through a first transistor;

cross-coupling a second transistor with the first transistor, where a size of the second transistor is a predetermined ratio to a size of the first transistor; and

sinking current from the external termination pad using the second transistor.



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20. The method of claim 19, the method further including the step of coupling a complex impedance between the external termination pad and a control terminal of the second transistor to control the slew rate of the amplifier.

21. The method of claim 15, where the step of amplifying a data signal with the amplifier to drive the external termination pad includes the steps of:

modulating the reference current with the data signal to produce a modulated current signal;

sinking the modulated current signal through a first transistor of a first pair;

cross-coupling a second transistor of the first pair with the first transistor of the first pair, where a size of the second transistor of the first pair is a predetermined ratio to a size of the first transistor of the first pair;

sinking current from the external termination pad using the second transistor of the first pair;

modulating the reference current with an inverted data signal, which is complementary to the data signal, to produce an inverted modulated current signal;

sinking the inverted modulated current signal through a first transistor of a second pair;

cross-coupling a second transistor of the second pair with the first transistor of the second pair, where a size of the second transistor of the second pair is the predetermined ratio to a size of the first transistor of the second pair; and

sinking current from an inverted external termination pad using the second transistor of the second pair.



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22. The method of claim 21, the method further including the step of coupling a first complex impedance between the external termination pad and a control terminal of the second transistor of the first pair and coupling a second complex impedance between the inverted external termination pad and a control terminal of the second transistor of the second pair to control the slew rate of the amplifier.

23. The method of claim 15, where the step of generating a current control signal by comparing a voltage at the external termination pad to the second reference voltage further comprises the steps of:

comparing the voltage at the external termination pad to the second reference voltage to produce an up/down signal; and

using the up/down signal to increase or decrease the current control signal.

24. The method of claim 23, where the step of comparing the voltage at the external termination pad to the second reference voltage to produce an up/down signal further includes:

scaling one of the terminating voltage and the first reference voltage using a resistance circuit; and

comparing another of the terminating voltage and the first reference voltage to the scaled one to obtain the second reference voltage.



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25. The method of claim 24, where the step of scaling one of the terminating voltage and the first reference voltage using another resistance circuit further includes the step of controlling an output swing of the amplifier by providing a selectably adjustable resistance in the resistance circuit.

26. The method of claim 23, where:

the step of using the up/down signal to increase or decrease the current control signal further includes increasing and decreasing a digital value of the current control signal responsive to the up/down signal; and

the step of sourcing an on-die termination current to the external termination pad that corresponds to the current control signal includes:

providing a plurality of transistors for sourcing current to the external termination pad, and

driving a control gate of each of the plurality of transistors with a corresponding bit of the digital value of the current control signal.

27. The method of claim 23, where:

the step of using the up/down signal to increase or decrease the current control signal further includes increasing and decreasing an analog value of the current control signal responsive to the up/down signal; and

the step of sourcing an on-die termination current to the external termination pad that corresponds to the current control signal includes:



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providing a plurality of transistors for sourcing current to the external termination pad, and

driving a control gate of each of the plurality of transistors with the analog value of the current control signal to operate the plurality of transistors in a linear operating range.

28. The method of claim 15, where the step of generating a current control signal by comparing a voltage at the external termination pad to the second reference voltage further comprises the steps of:

transmitting a predetermined data pattern at the external termination pad responsive to a transmit clock signal, the predetermined data pattern alternating between high and low logic voltage levels;

receiving, responsive to a receive clock signal, a data pattern at the external termination pad corresponding to the transmitted predetermined data pattern; and

comparing the received data pattern to the predetermined data pattern in order to generate an up/down signal configured to increase and decrease the current control signal according to the comparison between the received data pattern and the predetermined data pattern.

29. A device for interfacing to a bus through an external termination pad, the device comprising:

means for tracking a difference between a terminating voltage for the bus and a first reference voltage for the bus to produce a second reference voltage;



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means for generating a reference current that corresponds to the second reference voltage;

means for sourcing the reference current to an amplifier;

means for amplifying a data signal with the amplifier to drive the external termination pad;

means for generating a current control signal by comparing a voltage at the external termination pad to the second reference voltage; and

means for sourcing an on-die termination current to the external termination pad that corresponds to the current control signal.

30. The device of claim 29, where the means for tracking a difference between a terminating voltage for the bus and a first reference voltage for the bus to produce a second reference voltage further comprises:

means for scaling one of the terminating voltage and the first reference voltage using a resistance circuit;

means for comparing another of the terminating voltage and the first reference voltage to the scaled one to obtain a difference signal; and

where the means for sourcing the reference current to an amplifier includes means for driving a current source with the difference signal through the resistance circuit to the one of the terminating voltage and the first reference voltage.



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31. The device of claim 30, where the device further includes means for controlling an output swing of the amplifier by providing a selectably adjustable resistance in the resistance circuit.

32. The device of claim 30, where the means for sourcing the reference current to an amplifier includes means for mirroring the current through the current source to produce the reference current.

33. The device of claim 29, where the means for amplifying a data signal with the amplifier to drive the external termination pad includes:

means for modulating the reference current with the data signal to produce a modulated current signal;

means for sinking the modulated current signal through a first transistor;

means for multiplying the modulated current signal by cross-coupling a second transistor with the first transistor, where a size of the second transistor is a predetermined ratio to a size of the first transistor; and

means for sinking current from the external termination pad using the second transistor.

34. The device of claim 33, the device further including means for controlling a slew rate of the amplifier by introducing a complex impedance between the external termination pad and a control terminal of the second transistor.

35. The device of claim 29, where the means for amplifying a data signal with the amplifier to drive the external termination pad includes:

means for modulating the reference current with the data signal to produce a modulated current signal;

means for sinking the modulated current signal through a first transistor of a first pair;

means for multiplying the modulated current signal by cross-coupling a second transistor of the first pair with the first transistor of the first pair, where a size of the second transistor of the first pair is a predetermined ratio to a size of the first transistor of the first pair;

means for sinking current from the external termination pad using the second transistor of the first pair;

means for modulating the reference current with an inverted data signal, which is complementary to the data signal, to produce an inverted modulated current signal;

means for sinking the inverted modulated current signal through a first transistor of a second pair;

means for multiplying for multiplying the inverted modulated current signal by cross-coupling a second transistor of the second pair with the first transistor of the second pair, where a size of the second transistor of the second pair is the predetermined ratio to a size of the first transistor of the second pair; and

means for sinking current from an inverted external termination pad using the second transistor of the second pair.



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36. The device of claim 35, the device further including means for controlling the slew rate of the amplifier by coupling a first complex impedance between the external termination pad and a control terminal of the second transistor of the first pair and coupling a second complex impedance between the inverted external termination pad and a control terminal of the second transistor.

37. The device of claim 29, where the means for generating a current control signal by comparing a voltage at the external termination pad to the second reference voltage further comprises:

means for comparing the voltage at the external termination pad to the second reference voltage to produce an up/down signal; and

means for using the up/down signal to increase or decrease the current control signal.

38. The device of claim 37, where the means for comparing the voltage at the external termination pad to the second reference voltage to produce an up/down signal further includes:

means for scaling one of the terminating voltage and the first reference voltage using a resistance circuit; and

means for comparing another of the terminating voltage and the first reference voltage to the scaled one to obtain the second reference voltage.



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39. The device of claim 38, where the means for scaling one of the terminating voltage and the first reference voltage using another resistance circuit further includes means for controlling an output swing of the amplifier by providing a selectably adjustable resistance in the resistance circuit.

40. The device of claim 37, where:

the means for using the up/down signal to increase or decrease the current control signal further includes means for increasing and decreasing a digital value of the current control signal responsive to the up/down signal; and

the means for sourcing an on-die termination current to the external termination pad that corresponds to the current control signal includes:

means for providing a plurality of transistors for sourcing current to the external termination pad, and

means for driving a control gate of each of the plurality of transistors with a corresponding bit of the digital value of the current control signal.

41. The device of claim 37, where:

the means for using the up/down signal to increase or decrease the current control signal further includes means for increasing and decreasing an analog value of the current control signal responsive to the up/down signal; and

the means for sourcing an on-die termination current to the external termination pad that corresponds to the current control signal includes:



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means for providing a plurality of transistors for sourcing current to the external termination pad, and

means for driving a control gate of each of the plurality of transistors with the analog value of the current control signal to operate the plurality of transistors in a linear operating range.

42. The device of claim 29, where the means for generating a current control signal by comparing a voltage at the external termination pad to the second reference voltage further comprises:

means for transmitting a predetermined data pattern at the external termination pad responsive to a transmit clock signal, the predetermined data pattern alternating between high and low logic voltage levels;

means for receiving, responsive to a receive clock signal, a data pattern at the external termination pad corresponding to the transmitted predetermined data pattern; and

means for comparing the received data pattern to the predetermined data pattern in order to generate an up/down signal configured to increase and decrease the current control signal according to the comparison between the received data pattern and the predetermined data pattern.

43. A bus system, the bus system including:

at least one bus line;



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a termination voltage terminal coupled to the bus line and configured to have an external termination voltage;

a termination resistor coupled between the termination voltage terminal and the bus line and having an external resistance value; and

a bus interface device having an external termination pad coupled to the bus line, the bus interface device being configured to receive the termination voltage and an external reference voltage and compare the termination voltage and an external reference voltage in order to generate an output low reference voltage, the device being further configured to compare the output low reference voltage to a voltage at the external termination pad in order to generate a current control signal, where the device includes a current source configured to source current to the external termination pad responsive to the current control signal.

44. The bus system of claim 43, where the bus interface device is further configured to generate a reference current corresponding to the output low reference voltage and the device further includes an amplifier for generating an output signal at the external termination pad responsive to a data signal, where the amplifier operates from the reference current such that an output swing of the output signal of the amplifier corresponds to the output low reference voltage.

45. The bus system of claim 44, where the bus interface device further includes a scaling circuit for selectably adjusting the output low reference voltage in order to introduce asymmetry to the output swing of the output signal of the amplifier.



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46. The bus system of claim 43, where the bus interface device is further configured to generate the current control signal by transmitting a predetermined data pattern at the external termination pad, where the predetermined data pattern alternates between high and low logic levels, compare a signal present at the external termination pad to the output low reference voltage in order to obtain a received data pattern that corresponds to the transmitted predetermined data pattern, and compare the received data pattern to the predetermined data pattern in order to adjust the current control signal.

47. A current control circuit for a bus interface, the circuit comprising:

a first transistor having first and second current terminals and a control terminal, the first current terminal of the first transistor being coupled to a first power supply terminal and the control terminal of the first transistor being coupled to a circuit node configured to receive a first sampled logic voltage;

a first current source being coupled between the second current terminal of the first transistor and a second power supply terminal;

a second transistor having first and second current terminals and a control terminal, the first current terminal of the second transistor being coupled to the first power supply terminal and the control terminal of the second transistor being coupled to a circuit node configured to receive a second sampled logic voltage;

a second current source being coupled between the second current terminal of the second transistor and the second power supply terminal;

a third transistor having first and second current terminals and a control terminal, the second current terminal of the third transistor being coupled to the second power supply terminal;

a first resistor coupled between the control terminal of the third transistor and the second current terminal of the first transistor;

a second resistor coupled between the control terminal of the third transistor and the second current terminal of the second transistor;

a third current source being coupled between the first current terminal of the third transistor and the first power supply terminal;

a fourth transistor having first and second current terminals and a control terminal, the first current terminal of the fourth transistor being coupled to the first power supply terminal and the control terminal of the fourth transistor being coupled to a first external termination pad configured to receive a reference voltage;

a fourth current source being coupled between the second current terminal of the fourth transistor and the second power supply terminal;

a fifth transistor having first and second current terminals and a control terminal, the second current terminal of the fifth transistor being coupled to the second power supply terminal and the control terminal of the fourth transistor being coupled to the second current terminal of the fourth transistor;

a fifth current source being coupled between the first current terminal of the fifth transistor and the first power supply terminal; and

a comparator having inverting and non-inverting input terminals and an output terminal, the non-inverting input terminal being coupled to the first current terminal



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of the third transistor and the inverting terminal being coupled to the first current terminal of the fifth transistor, where the comparator is configured to compare the voltages received at the inverting and non-inverting input terminals and output a current control signal.

48. The current control circuit of claim 47, where the first, second and fourth transistors further comprise NMOS devices and the third and fifth transistors further comprise PMOS devices.

49. The current control circuit of claim 47, where the comparator further comprises:

a sixth transistor having first and second current terminals and a control terminal, the control terminal of the sixth transistor being coupled to the non-inverting terminal of the comparator and the first current terminal of the sixth transistor being coupled to an inverting output terminal of the comparator;

a first resistive load coupled between the first power supply terminal and the first current terminal of the sixth transistor;

a sixth current source coupled between the second current terminal of the sixth transistor and the second power supply terminal;

a seventh transistor having first and second current terminals and a control terminal, the control terminal of the seventh transistor being coupled to the inverting terminal of the comparator and the first current terminal of the seventh transistor being coupled to the output terminal of the comparator;



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a second resistive load coupled between the first power supply terminal and the first current terminal of the seventh transistor;

a seventh current source coupled between the second current terminal of the seventh transistor and the second power supply terminal;

an eighth current source coupled between the second current terminals of the sixth and seventh transistors and the second power supply terminal; and

an eighth transistor having first and second current terminals and a control terminal, the control terminal of the eighth transistor being configured to receive a first offset control signal, the first current terminal of the eighth transistor being coupled to the first power supply terminal, and the second current terminal of the eighth transistor being coupled to one of the output terminal of the comparator and the inverted output terminal of the comparator.

50. The current control circuit of claim 47, where the comparator further includes a ninth transistor having first and second current terminals and a control terminal, the control terminal of the ninth transistor being configured to receive a second offset control signal, the first current terminal of the ninth transistor being coupled to the first power supply terminal, and the second current terminal of the ninth transistor being coupled to another one of the output terminal of the comparator and the inverted output terminal of the comparator.



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51. A circuit for sensing an external resistance coupled to an external termination pad and adjusting a current drawn from the external termination pad, the circuit comprising:

an amplifier having inverting and non-inverting input terminals and an output terminal, the non-inverting input terminal being coupled to a circuit node configured to receive a reference voltage;

a first transistor having first and second current terminals and a control terminal, the control terminal of the first transistor being coupled to the output terminal of the first amplifier and the first current terminal of the first transistor being coupled to the inverting input terminal of the first amplifier;

a first resistive load coupled between the first current terminal of the first transistor and a circuit node configured to receive a termination voltage;

a second transistor having first and second current terminals and a control terminal, the control terminal of the second transistor being coupled to the first current terminal of the second transistor and the second current terminal of the first transistor and the second current terminal of the second transistor is coupled to a power supply terminal;

a third transistor having first and second current terminals and a control terminal, where the third transistor is larger than the second transistor by a selected ratio, and where the control terminal of the third transistor is coupled to the control terminal of the second transistor and the second current terminal of the third transistor is coupled to the power supply terminal;



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a second resistive load coupled between the first current terminal of the third transistor and the circuit node configured to receive the termination voltage;

a comparator having inverting and non-inverting input terminals and an output terminal, the inverting input terminal being coupled to the first current terminal of the third transistor and the non-inverting input terminal being coupled to the external termination pad;

a circuit node configured to receive a reference voltage;

a current logic control circuit having an input terminal coupled to the output terminal of the comparator and an output terminal for outputting the current control signal, where the current logic control circuit is configured to transform an output signal from the comparator into a current control signal; and

a current source coupled between the external termination pad and the power supply terminal, the current source being configured to receive the current control signal and conduct a current that is proportional to the current control signal.

52. A method for controlling current in a bus interface circuit, the method comprising the steps of:

charge coupling the circuit to a first node for receiving a first sampled logic voltage;

modulating a current from a first power supply terminal to a first circuit node responsive to the first sampled logic voltage;

charge coupling the circuit to a second node for receiving a second sampled logic voltage;



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modulating a current from the first circuit node to a second power supply terminal responsive to the second sampled logic voltage;

stepping up a voltage at the first circuit node to create a midrange voltage;

charge coupling the circuit to a third node for receiving a reference voltage;

modulating a current from the first power supply terminal to the second power supply terminal through a second circuit node responsive to the reference voltage;

stepping up a voltage at the second circuit node to create a stepped up reference voltage; and

comparing the midrange voltage and the stepped up reference voltage in order to generate a current control signal.

53. The method of claim 52, where the step of comparing the midrange voltage and the stepped up reference voltage in order to generate a current control signal further includes:

receiving a first offset signal; and

sourcing current from the first power supply terminal to the current control signal to offset the current control signal.

54. A method for sensing an external resistance coupled to an external termination pad and adjusting a current drawn from the external termination pad, the method comprising the steps of:

comparing a reference voltage to a termination voltage through a first resistive load;



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modulating a current between the termination voltage and a ground voltage through the first resistive load based upon the comparison to produce a first reference current;

mirroring the first reference current through a pair of transistors having a predetermined size ratio in order to produce a second reference current;

sinking the second reference current from the termination voltage through a second resistive load to produce an output low reference voltage;

comparing the output low reference voltage to a voltage at the external termination pad to produce a current control signal; and

sinking current from the external termination pad to the ground voltage responsive to the current control signal.

55. The method of claim 54, the method including the step of adjusting the first and second resistive loads in order to offset the current control signal.



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